IN THE CLAIMS:

Please amend the claims as follows:

1-7. (Cancelled)

8. (Currently amended) A semiconductor integrated circuit apparatus comprising:

an integrated circuit main body including a plurality of MOSFETs on a semiconductor substrate;

monitor means for monitoring at least one of the drain currents of said plurality of MOSFETs; and

a plurality of substrate voltage regulating means for regulating the substrate voltage of said semiconductor substrate so that said drain currents are constant,

wherein said monitor means comprises a constant current source and a monitoring MOSFET formed on the same substrate as said plurality of MOSFETs,

said substrate voltage regulating means comprises comparison means for comparing the source potential of said monitoring MOSFET with a predetermined reference potential with the drain terminal of said monitoring MOSFET and the drain terminals of said plurality of MOSFETs connected to ~~the ground~~ a predetermined potential, and

said substrate voltage regulating means feeds back the output voltage output based on the comparison result by said comparison means to the substrate voltage of said monitoring MOSFET.

9. (Original) The semiconductor integrated circuit apparatus according to claim 8, wherein said reference potential is a supply potential to the integrated circuit main body.

10. (Original) The semiconductor integrated circuit apparatus according to claim 8, wherein said substrate voltage regulating means outputs a voltage value obtained by providing,

by way of limiting means, the upper and lower limits of the output voltage output based on the comparison result of said comparison means.

11. (Original) The semiconductor integrated circuit apparatus according to claim 10, wherein said monitoring MOSFET is a p-type monitoring MOSFET, the upper limit of the output voltage value of said substrate voltage regulating means is set to a voltage equal to or above the supply potential of said integrated circuit main body and within a range where the GIDL effect does not occur in said p-type monitoring MOSFET, and the lower limit of the output voltage value of said substrate voltage regulating means is set to a voltage below the supply potential of said integrated circuit main body and within a range where said p-type monitoring MOSFET does not show the bipolar characteristics.

12. (Original) The semiconductor integrated circuit apparatus according to claim 10, wherein said monitoring MOSFET is an n-type monitoring MOSFET, the upper limit of the output voltage value of said substrate voltage regulating means is set to a voltage equal to or above the ground potential of said integrated circuit main body and within a range where said n-type monitoring MOSFET does not show the bipolar characteristics, and the lower limit of the output voltage value of said substrate voltage regulating means is set to a voltage below the ground potential of said integrated circuit main body and within a range where the GIDL effect does not occur in said n-type monitoring MOSFET.

13. (Original) The semiconductor integrated circuit apparatus according to claim 10, wherein the output of said limiting means is connected to voltage supply means for supplying a source voltage to said integrated circuit main body, and

said source voltage is raised when a substrate voltage is an upper limit voltage or more and said source voltage is lowered when the substrate voltage is a lower limit voltage or less.

14. (Original) The semiconductor integrated circuit apparatus according to claim 8, wherein said constant current source has a leakage current canceling MOSFET substantially identical in transistor size to said monitoring MOSFET,

when said leakage current canceling MOSFET is an n-type MOSFET, a source-drain current provided when the gate and drain of the n-type MOSFET have substantially the same potential is added, and

when said leakage current canceling MOSFET is a p-type MOSFET, a source-drain current provided when the gate and drain of the p-type MOSFET have substantially the same potential is added.

15. (Original) The semiconductor integrated circuit apparatus according to claim 14, wherein a well region that provides the substrate of said leakage current canceling MOSFET is separated from a well region that provides the substrate of said monitoring MOSFET.

16. (Original) The semiconductor integrated circuit apparatus according to claim 8, further comprising substrate voltage regulating means for regulating a substrate potential so that the individual threshold values of the plurality of MOSFETs become uniform, and

a voltage is applied to the gate of said monitoring MOSFET as the voltage value is changed in accordance with temperature so as to provide a more gradual gradient than the temperature gradient of said threshold values formed when a voltage applied to said gate is set to be constant.

17. (Original) The semiconductor integrated circuit apparatus according to claim 8, further comprising:

frequency-voltage conversion means, wherein a signal originating from a clock supplied to the integrated circuit main body is inputted to said frequency-voltage conversion means,

the frequency of said signal is converted into a voltage by said frequency-voltage conversion means, and

said voltage is applied to the gate of a MOSFET constituting said monitor means.

18-28. (Cancelled)

29. (Previously presented) The semiconductor integrated circuit apparatus according to claim 8, wherein said comparison means comprises: an operational amplifier to which the source potential of said monitoring MOSFET and the predetermined reference potential are input; and a push-pull circuit for outputting a voltage as an output voltage that is based on the comparison result of the source potential of said monitoring MOSFET and the predetermined reference potential in accordance with the output of said operational amplifier.

30. (Previously presented) The semiconductor integrated circuit apparatus according to claim 8, wherein said comparison means comprises an operational transconductance amplifier (OTA).

31. (New) The semiconductor integrated circuit apparatus according to claim 8, wherein said predetermined potential is a ground potential.

32. (New) The semiconductor integrated circuit apparatus according to claim 31, wherein said predetermined reference potential is a supply potential to the integrated circuit main body.

33. (New) The semiconductor integrated circuit apparatus according to claim 8, wherein said predetermined potential is a supply potential to the integrated circuit main body.

34. (New) The semiconductor integrated circuit apparatus according to claim 33, wherein said predetermined reference potential is a ground potential.